Title: Lab 1

Class: CMPEN 331

Name: Rachael Wilson

1. Your Verilog design code.

`timescale 1ns / 1ps

module dff3(input [2:0] ns, input clrn, input clk, output reg [2:0] q);

always @ (posedge clk)

begin

if (clrn == 1) begin

q <= ns;

end

else begin

q <= 3'b000;

end

end

endmodule

module counter(input [2:0] q, input u, output reg [2:0] ns,

output reg a, output reg b, output reg c, output reg d, output reg e, output reg f, output reg g );

always @(\*)

begin

if (u == 1) begin

if (q == 3'b101) begin

ns <= 3'b000;

end

else begin

ns <= q + 1;

end

end

else begin

if (q == 3'b000) begin

ns <= 3'b101;

end

else begin

ns <= q - 1;

end

end

case(q)

3'b000: begin

g=1'b1; f=1'b0; e=1'b0; d=1'b0; c=1'b0; b=1'b0; a=1'b0;

end

3'b001: begin

g=1'b1; f=1'b1; e=1'b1; d=1'b1; c=1'b0; b=1'b0; a=1'b1;

end

3'b010: begin

g=1'b0; f=1'b1; e=1'b0; d=1'b0; c=1'b1 ;b=1'b0; a=1'b0;

end

3'b011: begin

g=1'b0; f=1'b1; e=1'b1; d=1'b0; c=1'b0; b=1'b0; a=1'b0;

end

3'b100: begin

g=1'b0; f=1'b0; e=1'b1; d=1'b1; c=1'b0; b=1'b0; a=1'b1;

end

3'b101: begin

g=1'b0; f=1'b0; e=1'b1; d=1'b0; c=1'b0; b=1'b1; a=1'b0;

end

endcase

end

endmodule

1. Your Verilog® Test Bench design code (use the test sequence shown in Figure 6). Add “`timescale 1ns/1ps” as the first line of your test bench file.

`timescale 1ns / 1ps

module testbench();

reg clrn\_tb;

reg clk\_tb;

reg u\_tb;

wire [2:0] q\_tb;

wire [2:0] ns\_tb;

wire a,b,c,d,e,f,g;

dff3 dff3\_tb(ns\_tb, clrn\_tb, clk\_tb, q\_tb);

counter counter\_tb(q\_tb, u\_tb, ns\_tb, a, b, c, d, e, f, g);

initial begin

clrn\_tb = 0;

clk\_tb = 1;

u\_tb = 1;

#1 clrn\_tb = 1;

#16 u\_tb = 0;

end

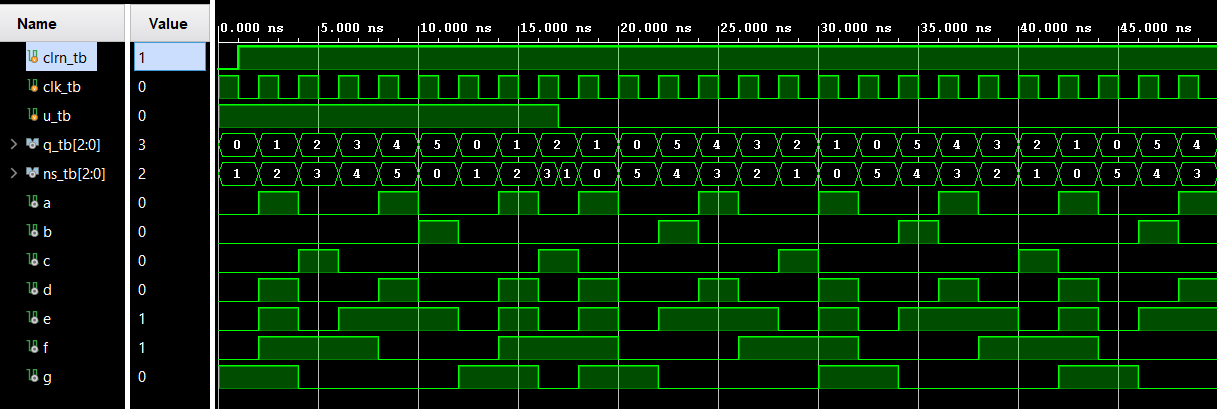
always begin

#1;

clk\_tb = ~clk\_tb;

end

endmodule

1. The waveforms resulting from the verification of your design with ModelSim showing all the outputs of the following signals (q, a, b, c, d, e, f, g).
2. The design schematics from the Xilinx synthesis of your design. Do not use any area constraints. A screenshot of a computer

   Description automatically generated
3. Snapshot of the I/O Planning andA screenshot of a computer

   Description automatically generated
4. Snapshot of the floor planning

A screenshot of a video game

Description automatically generated